

Remarks

Claims 1-20 are pending. Reconsideration and allowance in view of the above amendments and following remarks are respectfully requested.

In response to the objection to the specification, Applicants have herein amended paragraph [0008] and added new paragraph [0018.1]. Applicants respectfully submit that the remaining changes proposed by the Examiner are not necessary, and respectfully decline to make such changes in the patent application.

FIGS. 1 and 2 have been amended to include the legend "PRIOR ART."

Claim 20 has been amended to correct a typographical error.

Claims 4-6, 11-13, and 17-19 are objected to as being dependent upon a rejected base, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

Claims 1-3, 8-10, and 14-16 are rejected under 35 U.S.C. 103(a) over Kellam et al. (U.S. 5,702,686), hereafter "Kellam," in view of the paper to Zhu et al. entitled "Package Clock

Distribution Design Optimization for High-Speed and Low-Power VLSIs," hereafter "Zhu." Claims 7 and 20 are rejected under 35 U.S.C. 103(a) over Kellam and Zhu and further in view of Minami (U.S. 2004/0090282). These rejections are defective because the cited references, take alone or in any combination, fail to teach or suggest each and every feature set forth in the claims as required by 35 U.S.C. 103(a).

Regarding independent claim 1 (and similarly independent claims 8 and 14), the Examiner admits that Kellam fails to teach or suggest the claimed steps of "scanning the route paths for transmission line replacement candidates," and "for each transmission line replacement candidate, automatically selecting a buffered wire or a transmission line to implement the route path." To overcome this glaring deficiency of Kellam, the Examiner relies on the teachings of Zhu. In particular, the Examiner alleges that the "route paths between the ASIC are examined (i.e., scanned) to determine route paths in clock trees for transmission line replacement candidates in order to construct global clock trees using transmission line thereby achieving high-speed and low-power performance of the ASIC." Applicants respectfully disagree with the Examiner's analysis and conclusion regarding Zhu.

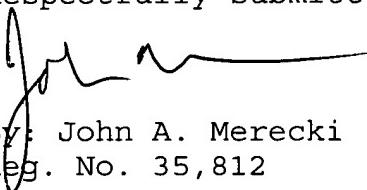
Zhu discloses a technique whereby global clock trees are

routed through a package layer within the package of an integrated circuit to take advantage of the lower resistance and capacitance of the larger and thicker wires typically used in the package layer. (Page, 56, col. 2, lines 30-40.) Local clock trees (i.e., those clock trees located within the integrated circuit itself), however, are provided in a conventional manner. This is illustrated in FIG. 2(a) of Zhu where a single-chip package is used to couple a flip chip (i.e., an integrated circuit) to a substrate (e.g., printed circuit board) (not shown), wherein a global clock tree is routed on package to take advantage of the package's wider and thicker wiring. Contrary to the claimed invention, however, interconnects (e.g., local clock trees, route paths between blocks of ASICs, etc.) within the flip chip itself are not scanned for transmission line replacement candidates, nor is a selection made between a buffered wire or a transmission line to implement route paths comprising transmission line replacement candidates within the flip chip. Clearly, therefore, the Examiner's assertion that "route paths between the ASIC are examined (i.e., scanned) to determine route paths in clock trees for transmission line replacement candidates in order to construct global clock trees using transmission line thereby achieving high-speed and low-power performance of the ASIC," is incorrect.

Accordingly, Applicants submit that independent claims 1, 8, and 14 and their associated dependent claims 2-7, 9-13, and 15-20, respectively, are allowable.

If the Examiner believes that any further discussion of the invention would be helpful, Applicants' representative is available at (518) 449-0044, and earnestly solicits such discussion.

Respectfully submitted,



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Date: 12/9/04

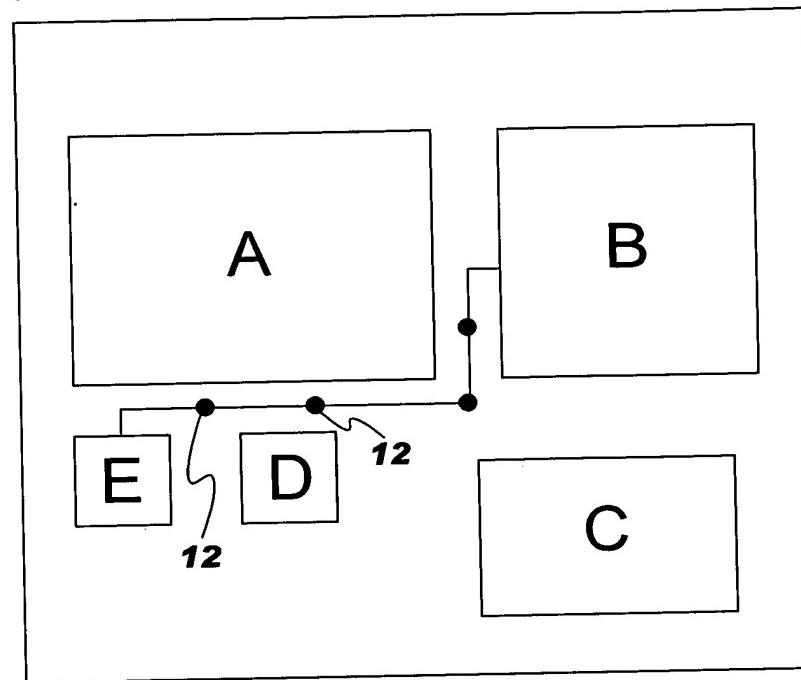
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Amendments to the Drawings

Please amend FIGS. 1 and 2 to include the legend "PRIOR ART."

ANNOTATED SHEET

1/3
FIG. 1 PRIOR ART



10
FIG. 2 PRIOR ART

